Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **V+**
2. **NC**
3. **INPUT 1**
4. **INPUT 2**
5. **NC**
6. **V-**
7. **NC**
8. **STROBE 2**
9. **OUTPUT 2**
10. **GND**
11. **OUTPUT 1**
12. **NC**
13. **STROBE 1**
14. **VCC**

**.038”**

**.055”**

**MASK**

**REF**

**LM**

**161**

**E**

**3**

**4**

**6 8 9 10**

**13**

**11**

**1 14**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Floating**

**Mask Ref: LM161E**

**APPROVED BY: DK DIE SIZE .038” X .055” DATE: 11/11/21**

**MFG: NATIONAL SEMI THICKNESS .015” P/N: LM361**

**DG 10.1.2**

#### Rev B, 7/19/02